ABSTRACT

A method for controlling functional units in a processor, according to which in a configuration a sequence of primary instruction words which consists of several instruction word parts and originates from a translation of a program code is compressed and stored as a sequence of associated program words. The invention also relates to a processor system for carrying out this method. The aim of the invention is to increase operating speed in an application-specific manner while retaining a low program word width. To this end, as regards the method, a program word contains a first characteristic of a primary instruction word and instruction word parts which differentiate the primary instruction word belonging to the program word from the primary instruction word belonging to the characteristic. By means of the first characteristic contained in the program word a secondary instruction word is generated by exchanging the instruction word parts contained in the program word with those in a preceding secondary instruction word. On the system side the aim of the invention is solved by providing for the instruction word buffer to consists of a memory with optional line-by-line access.